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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/535,060
Filing Date: May 13, 2005
Appellant(s): MEEUSEN, RAFAEL

Michael Ure
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/13/08 appealing from the Office action mailed 12/14/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. Claim 4 is rejected under 35 USC 102(b) as being anticipated by Therssen et al.

As a result, the grounds of rejection presented for review on appeal are:

Claims 1-10 stand rejected under 35 USC 102(b) as being anticipated by Wildhagen.

Claim 1 stands rejected under 35 USC 102(b) as being anticipated by Therssen.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

7,149,312	WILDHAGEN	12-2006
EP0512606	THERSSEN	7-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

9.1 Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wildhagen (US007149312B1).

Regarding claim 9, Wildhagen discloses, in Fig. 5, a stereo decoder in a receiver with a frequency demodulator circuit (col. 1, lines 13-15), wherein the stereo decoder comprises two frequency shifting circuits connected is series with one another (e.g. elements 37 and 20 are connected in series). The term “shifting”, according to dictionary, means varying. So the claimed “frequency shifting circuit” could read on a circuit that varies the input frequency and generates an output with a varied frequency. This varied frequency is different from the input frequency. Element 37 varies the frequency of the input (the output of element 14). The output of element 37 has a frequency ω_{pil}. The output of element 20 has a frequency of audio spectrum defined by the stereo difference signal.

Regarding claims 1 and 2, Wildhagen discloses, in Fig. 5, a method for a receiver having a signal path incorporating a tuner, a frequency demodulator circuit (although the

tuner and frequency demodulator circuit are not explicitly shown, they are inherently included) for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier (col. 1, lines 9-16), a sampler (14) for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder (Fig. 5) for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal, wherein the analog stereo multiplex signal is converted into a time discrete digital stereo multiplex signal and then the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz (37) to extract at least one of the time-discrete digital sum and the time discrete digital stereo difference signal (through 20, 21, 24), and further shifted (by 18) and having a lowpass filter (21 or 24). Again, the term “shifting”, according to dictionary, means varying. So the claimed “is shifted over a frequency of 19 kHz” could read on a circuit that varies the input frequency and generates an output with a 19 kHz to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal. This varied frequency is different from the input frequency.

Regarding claim 3, the claimed complex filter reads on element 21.

Regarding claim 4, Wildhagen shows the second low pass filter (15) and the path from 15 to 16 is parallel to the path from 20, 21 and 24.

Regarding claim 5, Wildhagen discloses a receiver having a signal path incorporating a tuner, a frequency demodulator circuit (although not explicitly shown,

they are inherently included) for supplying an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier (col. 1, lines 9-16), a sampler (14) for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder (Fig. 5) for decoding the time discrete digital stereo multiplex signal into a time discrete digital stereo sum and a time discrete digital stereo difference signal, wherein the stereo decoder comprises two frequency shifting circuits connected in series with one another (e.g. 37 and 20). The term "shifting", according to dictionary, means varying. So the claimed "frequency shifting circuit" means a circuit that varies the input frequency and generates an output with a varied frequency. This varied frequency is different from the input frequency. Element 37 varies the frequency of the input (the output of element 14). The output of element 37 has a frequency ω_{pil}. The output of element 20 has a frequency of audio spectrum defined by the stereo difference signal.

Regarding claim 6, Wildhagen shows the low pass filter (21 or 24 in Fig. 5).

Regarding claim 7, Wildhagen shows the complex filter (21 or 24 in Fig. 5).

Regarding claim 8, Wildhagen shows the second low pass filter (15).

9.2 Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Therssen et al (hereafter Therssen) (EP000512606B1).

Regarding claim 1, Therssen discloses a method for a receiver (Fig. 1) having a signal path incorporating a tuner (T), a frequency demodulator circuit (FD) for supplying

an analog stereo multiplex signal comprising a baseband stereo sum signal, a 19 kHz stereo pilot and a stereo difference signal, which is double sideband amplitude-modulated on a suppressed 38 kHz subcarrier, a sampler (A/D) for converting the analog stereo multiplex signal into a time discrete digital stereo multiplex signal and a stereo decoder (SD) for decoding the time discrete digital stereo multiplex signal into a time-discrete digital stereo sum and a time discrete digital stereo difference signal; wherein the analog stereo multiplex signal is converted into a time discrete digital stereo multiplex signal and then the time discrete digital stereo multiplex signal is shifted over a frequency of 19 kHz (by M2; the signal SMO represents the discrete digital stereo multiplexed signal; col. 6, line 35) to extract at least one of the time-discrete digital stereo sum and the time discrete digital stereo difference signal (see Fig. 2 for extracting the difference signal and the sum signal using SMO, and decode L+R and L-R to obtain L and R).

(10) Response to Argument

On p. 10, appellant argued that the DPLL circuit does not perform any frequency shifting of the time discrete digital stereo multiplex signal m itself. This is not persuasive. Appellant fails to explain the term “frequency shifting” in the argument. Examiner interpreted the term based on the dictionary definition of the word “shifting”. The term “shifting”, according to dictionary, means varying. So the claimed “frequency shifting circuit” could read on a circuit that varies the input frequency and generates an output with a varied frequency. This varied frequency is different from the input

frequency. As illustrated in Fig. 5, Wildhagen shows that the discrete digital stereo multiplex signal (after the element 14) is shifted over a frequency of 19 kHz (the output of DPLL has a frequency of 19 kHz; the discrete digital stereo multiplex signal includes signal at 38 kHz) to extract the stereo difference signal (through 18, 20, 21 and 24).

On p. 10, appellant argued that the DPLL circuit of Wildhagen cannot be considered to be "two frequency shifting circuits connected in series with one another as specified in claim 9. Examiner disagrees. Claim 5 has a similar language as claim 9. So Examiner would address the argument for both claims 5 and 9. Claims 5 and 9 specify that a stereo decoder comprises two frequency shifting circuits connected in series with one another. Neither claim 5 nor claim 9 explicitly state what signal is being applied to the two frequency shifting circuits connected in series with one another. Furthermore, it is noted that the features upon which applicant relies (i.e., to shift the center frequency of an information-bearing signal, not a carrier signal or reference signal) is not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

On p. 9, appellant argued that M2 in Therssen does not shift the time discrete digital stereo multiplex signal over a frequency of 19 kHz to extract at least one of the time-discrete digital stereo sum and time discrete digital stereo difference signal because M2 is used to determine whether a mono or stereo output. First of all, mono in Therssen is the stereo sum signal. The stereo sum signal is extracted after MSS. MSS is controlled by 19 kHz generated by DIV. The term “shifting”, according to dictionary,

means varying. So the claimed "frequency shifting" could read on the frequency of the input signal being varied that the output has a varied frequency. This varied frequency is different from the input frequency. The signal after DIV is 19 kHz which is generated by varying the input frequency on the signal SMO. The stereo sum signal is extracted by varying the SMO over a frequency of 19 kHz.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

pwl

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